PATENT
Attorney Docket No.: K35A1303

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
QUOC N. DANG et al.

Application No.: 10/628,144

Filed: July 28, 2003

For: CLUSTER-BASED CACHE MEMORY ALLOCATION

Group Art Unit: 2187

Examiner: Peugh, Brian R.



DECLARATION OF QUOC N. DANG
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Quoc N. Dang, hereby declare as follows:

1. I am a joint inventor in parent application number 09/552,407 (the "Parent Application"), now patent number 6,606,682, and I am a joint inventor in this continuation application number 10/628,144 (the "Continuation Application") which claims priority to the Parent Application. I am making this declaration to establish facts showing that the invention claimed in this Continuation Application was reduced to practice before January 25, 2000, which I am informed is the issue date of U.S. Patent Number 6,018,789 to Sokolov et al. (the "Sokolov '789 patent"). I will hereinafter refer to January 25, 2000 as the "Effective Date" of the Sokolov '789 patent.

2. I was employed by the original assignee, Western Digital Corporation ("WDC") at WDC's Irvine facility in the State of California, during th time between my

conception of the invention recited in claims 1, 2, 6-9 and 13-20, which claims are being pursued in this Continuation Application, and the filing of the Parent Application.

3. I have read claims 1, 2, 6-9 and 13-20 and have a technical understanding of how such claims relate to the disclosure of the Parent Application and this Continuation Application.

4. I helped develop and reduce to practice, in the United States of America, a hard disk drive having an integrated circuit to which claims 1, 2, 6-9 and 13-20 apply prior to the Effective Date of the Sokolov '789 patent. This particular disk drive was called "Rebel" during its development. The Rebel disk drive, as reduced to practice, included a cache memory and a cache control system for implementing a cache method. The cache memory had a plurality of sequentially-ordered memory clusters for caching disk data of disk sectors identified by logical block addresses. The cache control system had a plurality of cluster control blocks and a tag memory including a plurality of tag records. Each cluster control block had a cluster segment record for associating the cluster control block with a particular memory cluster and for forming variable length segments of the memory clusters without regard to the sequential order of the memory clusters. Each tag record assigned a segment to a contiguous range of logical block addresses and defined the cluster control blocks forming the segment. Each segment of the memory clusters was for caching disk data of the assigned contiguous range of logical block addresses. The cluster segment record of each cluster control block associated with a segment included a pointer to a subsequent cluster control block or to indicate an end cluster control block of the segment. The cache control system of the Rebel disk drive also included a microprocessor that de-allocated an existing assigned segment and assigned the segment's associated cluster control blocks to the free list if a sufficient number of cluster control blocks were not available on the free list to enable caching of a range of logical block addresses requested by a host command. Also, the memory clusters were uniformly sized. Further, the cache memory was separate from the tag memory.

5. Attached hereto as Exhibit "A" is an assembly tree of a Rebel disk drive. The Rebel disk drive included an ASSEMBLY PCB 61-600840-XXX (see arrow). The assembly tree is dated before the Effective Date of the Sokolov '789 patent (see revision dates in the upper right hand corner).

6. Attached hereto as Exhibit "B" is a Bill of Materials Report for an ASSEMBLY PCB 61-600840-001, which includes an integrated circuit: IC WD70C10SW/I285S (see arrow on page 2).

7. Attached hereto as Exhibit "C" are a Title page (page 1) and a select portion of a Table of Contents (pages 8-10) of a Device Specification for the integrated circuit IC WD70C10SW/I285S. The integrated circuit includes the cache control system (see arrow pointing to heading 10 on page 8) and the tag memory (see arrow pointing to heading 11 on page 9) that enable the Rebel disk drive to implement the cache method. The Device Specification is dated before the Effective Date of the Sokolov '789 patent.

9. This declaration factually establishes that the claimed invention was reduced to practice in the United States before the Effective Date of the Sokolov '789 patent.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application and any patent issuing thereon.

Date: October 13, 2003

Lake Forest, California
(city)

Quoc N. Dang

PATENT
Attorney Docket No.: K35A1303

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
QUOC N. DANG et al.

Application No.: 10/628,144

Filed: July 28, 2003

For: CLUSTER- BASED CACHE MEMORY ALLOCATION

Group Art Unit: 2187

Examiner: Peugh, Brian R.



DECLARATION OF TSUN Y. NG
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Tsun Y. Ng, hereby declare as follows:

1. I am a joint inventor in parent application number 09/552,407 (the "Parent Application"), now patent number 6,606,682, and I am a joint inventor in this continuation application number 10/628,144 (the "Continuation Application") which claims priority to the Parent Application. I am making this declaration to establish facts showing that the invention claimed in this Continuation Application was reduced to practice before January 25, 2000, which I am informed is the issue date of U.S. Patent Number 6,018,789 to Sokolov et al. (the "Sokolov '789 patent"). I will hereinafter refer to January 25, 2000 as the "Effective Date" of the Sokolov '789 patent.

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conception of the invention recited in claims 1, 2, 6-9 and 13-20, which claims are being pursued in this Continuation Application, and the filing of the Parent Application.

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5. Attached hereto as Exhibit "A" is an assembly tree of a Rebel disk drive. The Rebel disk drive included an ASSEMBLY PCB 61-600840-XXX (see arrow). The assembly tree is dated before the Effective Date of the Sokolov '789 patent (see revision dates in the upper right hand corner).

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10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application and any patent issuing thereon.

Date: ~~September~~ OCTOBER 13, 2003

ORANGE, California
(city)

Tsun Y. Ng

PATENT
Attorney Docket No.: K35A1303

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
QUOC N. DANG et al.

Application No.: 10/628,144

Filed: July 28, 2003

For: CLUSTER-BASED CACHE MEMORY ALLOCATION

Group Art Unit: 2187

Examiner: Peugh, Brian R.



DECLARATION OF RALPH H. CASTRO
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Ralph H. Castro, hereby declare as follows:

1. I am a joint inventor in parent application number 09/552,407 (the "Parent Application"), now patent number 6,606,682, and I am a joint inventor in this continuation application number 10/628,144 (the "Continuation Application") which claims priority to the Parent Application. I am making this declaration to establish facts showing that the invention claimed in this Continuation Application was reduced to practice before January 25, 2000, which I am informed is the issue date of U.S. Patent Number 6,018,789 to Sokolov et al. (the "Sokolov '789 patent"). I will hereinafter refer to January 25, 2000 as the "Effective Date" of the Sokolov '789 patent.

2. I was employed by the original assignee, Western Digital Corporation ("WDC") at WDC's Irvine facility in the State of California, during the time between my

conception of the invention recited in claims 1, 2, 6-9 and 13-20, which claims are being pursued in this Continuation Application, and the filing of the Parent Application.

3. I have read claims 1, 2, 6-9 and 13-20 and have a technical understanding of how such claims relate to the disclosure of the Parent Application and this Continuation Application.

4. I helped develop and reduce to practice, in the United States of America, a hard disk drive having an integrated circuit to which claims 1, 2, 6-9 and 13-20 apply prior to the Effective Date of the Sokolov '789 patent. This particular disk drive was called "Rebel" during its development. The Rebel disk drive, as reduced to practice, included a cache memory and a cache control system for implementing a cache method. The cache memory had a plurality of sequentially-ordered memory clusters for caching disk data of disk sectors identified by logical block addresses. The cache control system had a plurality of cluster control blocks and a tag memory including a plurality of tag records. Each cluster control block had a cluster segment record for associating the cluster control block with a particular memory cluster and for forming variable length segments of the memory clusters without regard to the sequential order of the memory clusters. Each tag record assigned a segment to a contiguous range of logical block addresses and defined the cluster control blocks forming the segment. Each segment of the memory clusters was for caching disk data of the assigned contiguous range of logical block addresses. The cluster segment record of each cluster control block associated with a segment included a pointer to a subsequent cluster control block or to indicate an end cluster control block of the segment. The cache control system of the Rebel disk drive also included a microprocessor that de-allocated an existing assigned segment and assigned the segment's associated cluster control blocks to the free list if a sufficient number of cluster control blocks were not available on the free list to enable caching of a range of logical block addresses requested by a host command. Also, the memory clusters were uniformly sized. Further, the cache memory was separate from the tag memory.

5. Attached hereto as Exhibit "A" is an assembly tree of a Rebel disk drive. The Rebel disk drive included an ASSEMBLY PCB 61-600840-XXX (see arrow). The assembly tree is dated before the Effective Date of the Sokolov '789 patent (see revision dates in the upper right hand corner).

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10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application and any patent issuing thereon.

Date: October 13, 2003

Chandler, Arizona
(city)

Ralph H. Castro

PATENT
Attorney Docket No.: K35A1303

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
QUOC N. DANG et al.

Application No.: 10/628,144

Filed: July 28, 2003

For: CLUSTER- BASED CACHE MEMORY ALLOCATION

Group Art Unit: 2187

Examiner: Peugh, Brian R.



DECLARATION OF VIRGIL V. WILKINS
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Virgil V. Wilkins, hereby declare as follows:

1. I am a joint inventor in parent application number 09/552,407 (the "Parent Application"), now patent number 6,606,682, and I am a joint inventor in this continuation application number 10/628,144 (the "Continuation Application") which claims priority to the Parent Application. I am making this declaration to establish facts showing that the invention claimed in this Continuation Application was reduced to practice before January 25, 2000, which I am informed is the issue date of U.S. Patent Number 6,018,789 to Sokolov et al. (the "Sokolov '789 patent"). I will hereinafter refer to January 25, 2000 as the "Effective Date" of the Sokolov '789 patent.

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QUOC N. DANG et al.
Application No.: 10/628,144
Filed: July 28, 2003
Page 2

PATENT
Docket No.: K35A1303

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In re Application of:
QUOC N. DANG et al.
Application No.: 10/628,144
Filed: July 28, 2003
Page 3

PATENT
Docket No.: K3SA1303

5. Attached hereto as Exhibit "A" is an assembly tree of a Rebel disk drive. The Rebel disk drive included an ASSEMBLY PCB 61-600840-XXX (see arrow). The assembly tree is dated before the Effective Date of the Sokolov '789 patent (see revision dates in the upper right hand corner).

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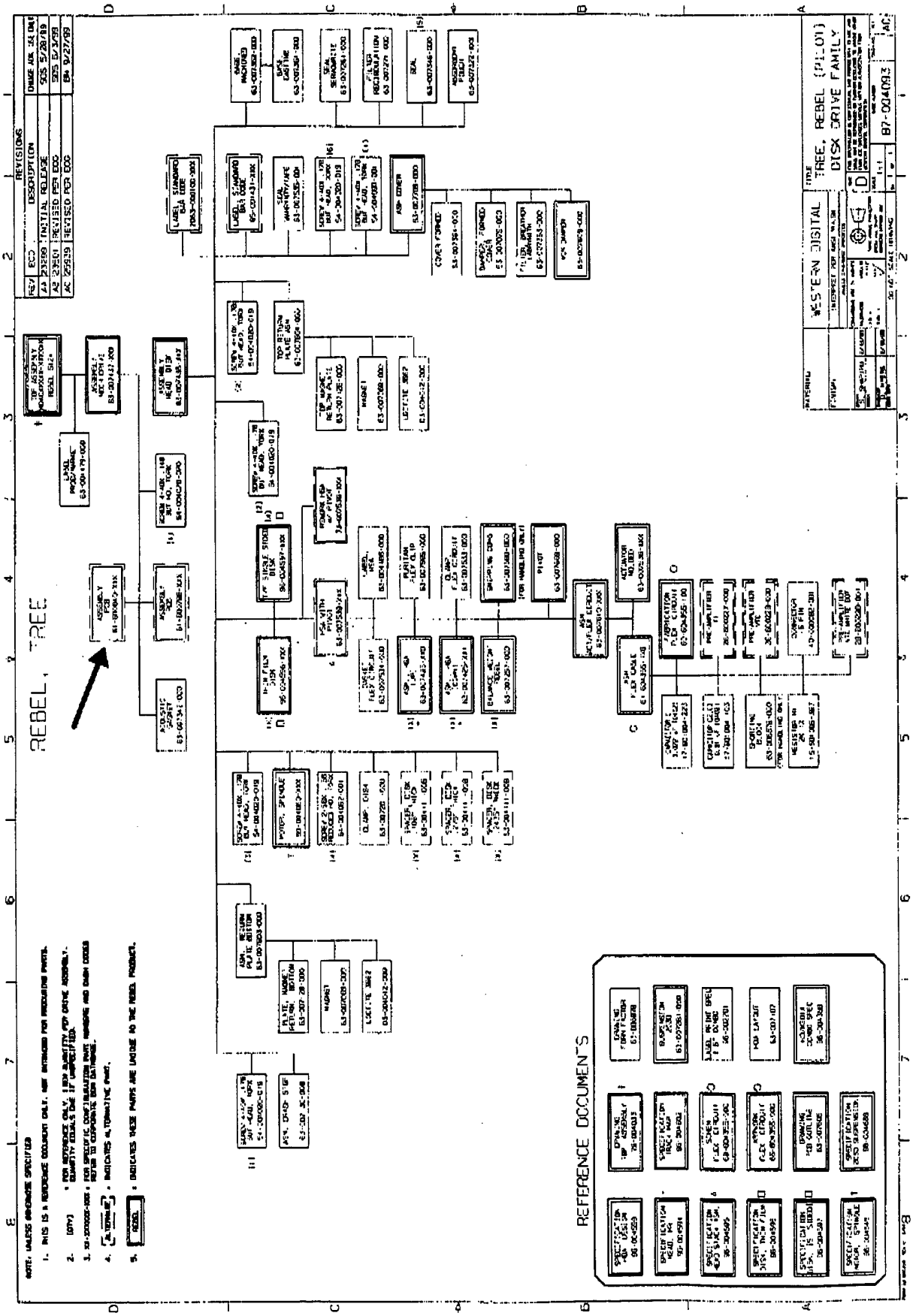
Date: October 17, 2003

Perris, California
(city)

Virgil V. Wilkins

# Exhibit A



# Exhibit B



WD Bill of Materials Report (Web) Report Date: Sat, 15 Mar 2003 00:37:33 GMT

Item: 61-600840-001 Rev: E as of 15-MAR-2003 00:37:34 GMT Org ID:WDC
Desc: PCBA, REBEL ENTEK FLASH

| Seq | Item Number | Description | Rev | Qty | Ref Des |
|---|---|---|---|---|---|
| 1 | 60-600840-000 | PCB ENTEK REBEL / REBEL 2 | A | 1 | |
| | 60-600840-400 | PCB, REBEL / REBEL 2 ENTEK 4UP PANEL | | 1 | |
| | 60-600840-X00 | PCB, REBEL / REBEL 2 ENTEK CROSSOUT PANEL | | 1 | |
| 3 | 15-600003-000 | RES CM 0.0 OHM 1/10W 0805 | A | 1 | R22 |
| 4 | 15-600004-000 | RES CM 0.0 OHM 1/16W 0603 | A | 4 | R34 R38 R41 R57 |
| 8 | 15-600004-345 | RES CM 10 OHM 5% 1/16W 0603 | A | 1 | R21 |
| 10 | 15-601004-263 | RES CM 80.6 OHM 1% 1/16W 0603 | A | 2 | R12 R13 |
| 12 | 15-600004-357 | RES CM 33 OHM 5% 1/16W 0603 | A | 3 | R17 R39 R46 |
| 15 | 15-600004-363 | RES CM 56 OHM 5% 1/16W 0603 | A | 2 | R20 R37 |
| 17 | 15-600004-369 | RES CM 100 OHM 5% 1/16W 0603 | A | 7 | R23 R29 R3 R30 R35 R4 R40 |
| 18 | 15-600004-376 | RES CM 200 OHM 5% 1/16W 0603 | A | 6 | R10 R15 R16 R26 R31 R33 |
| 19 | 15-600004-385 | RES CM 470 OHM 5% 1/16W 0603 | A | 2 | R18 R43 |
| 20 | 15-600004-393 | RES CM 1.0K 5% 1/16W 0603 | A | 2 | R47 R48 |
| 23 | 15-600004-400 | RES CM 2.0K 5% 1/16W 0603 | A | 3 | R49 R50 R51 |
| 24 | 15-600004-417 | RES CM 10K 5% 1/16W 0603 | A | 7 | R1 R14 R25 R36 R45 R69 R9 |
| 26 | 15-600004-441 | RES CM 100K 5% 1/16W 0603 | A | 1 | R2 |
| 29 | 15-600004-449 | RES CM 220K 5% 1/16W 0603 | A | 2 | R5 R70 |
| 31 | 15-600004-489 | RES CM 10M 5% 1/16W 0603 | A | 1 | R65 |
| 33 | 15-601001-767 | RES CM 1.50 OHM 1% 1/4W 1206 | A | 2 | R67 R68 |
| 34 | 15-601004-301 | RES CM 200 OHM 1% 1/16W 0603 | A | 1 | R19 |
| 35 | 15-601004-416 | RES CM 3.16K 1% 1/16W 0603 | A | 1 | R64 |
| 36 | 15-601004-423 | RES CM 3.74K 1% 1/16W 0603 | A | 1 | R62 |
| 37 | 15-601004-431 | RES CM 4.53K 1% 1/16W 0603 | A | 1 | R11 |
| 39 | 15-601004-464 | RES CM 10.0K 1% 1/16W 0603 | A | 1 | R55 |
| 42 | 15-601004-560 | RES CM 100K 1% 1/16W 0603 | A | 1 | R58 |
| 43 | 15-601004-625 | RES CM 475K 1% 1/16W 0603 | A | 1 | R56 |
| 45 | 17-601002-333 | CAP CER .033UF 10% X7R 0805 | A | 1 | C49 |
| 49 | 17-600003-101 | CAP CER 100PF 5% NPO 50V 0603 | A | 4 | C16 C17 C30 |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | C51 |
| 50 | 17-600003-150 | CAP CER 15PF 5% NPO 50V 0603 | A | 2 | C29 C40 |
| 51 | 17-600003-181 | CAP CER 180PF 5% NPO 50V 0603 | A | 1 | C43 |
| 52 | 17-600003-221 | CAP CER 220pF 5% NPO 0603 | A | 1 | C63 |
| 53 | 17-600003-391 | CAP CER 390pF 5% NPO 25V 0603 | A | 2 | C32 C33 |
| 55 | 17-601003-104 | CAP CER 0.1UF 10% X7R 16V 0603 | A | 1 | C62 |
| 57 | 17-601003-332 | CAP CER 3300PF 10% X7R 50V 0603 | A | 10 | C11 C15 C19 C21 C27 C28 C34 C39 C4 C6 |
| 58 | 17-601003-154 | CAP CER 0.15UF X7R 10% 10V 0603 | A | 1 | C9 |
| 59 | 17-602003-104 | CAP CER 0.1UF +80-20% Y5V 25V 0603 | A | 19 | C1 C12 C14 C18 C2 C20 C22 C3 C37 C41 C42 C44 C45 C46 C50 C56 C58 C60 C8 |
| 60 | 17-603006-105 | CAP CER 1.0UF X7R 20% 16V 1206 | A | 2 | C31 C35 |
| 61 | 19-600000-194 | CAP TANT 10UF 20% 10V (A) | A | 1 | C57 |
| 62 | 19-600000-193 | CAP TANT 4.7UF 20% 10V (A) | A | 1 | C5 |
| 63 | 19-600000-195 | CAP TANT 22uF 20% 10V (B) | A | 1 | C47 |
| 69 | 19-602000-160 | CAP TANT 1.0UF 20% 35V (B) | D | 1 | C52 |
| 70 | 19-602000-167 | CAP TANT 15uF 20% 35V (D) | A | 1 | C48 |
| 72 | 27-600099-000 | IC FLASH 64K*16 35NS 44PLCC | A | 1 | U2 |
| | 43-600065-001 | SCKT IC 44PLCC W/O KEY .185H MAX | | 1 | |
| 75 | 27-601123-000 | IC SDRAM 1M*16-10 SYNC 50TSOP | A | 1 | U4 |
| 77 | 28-601018-000 | IC LM1117B 3.3V 1.2A 2% REG DPAK | A | 1 | U6 |
| 78 | 28-601012-000 | IC 78M08 8V 2% REG D-PAK | A | 1 | U7 |
| 80 | 29-600506-000 | IC L6262 R2.4 ORCA 44TQFP | A | 1 | U5 |
| | 29-600528-000 | IC L6262 R2.6 ORCA 44TQFP | | 1 | |
| 82 | 29-600507-000 | IC CLSH3367 R=B2 RIGEL II 100MQFP | A | 1 | U3 |
| | 2029-001003-000 | IC CLSH3367 R=B3 RIGEL II DPH 100MQFP | | 1 | |
| | 29-600508-000 | IC CLSH3367DH-B2 RIGEL-2 100MQFP | | 1 | |
| 84 | 29-601226-000 | IC WD70C10SW/I285S R=3.0 176TQFP | A | 1 | U1 |
| 86 | 31-600043-000 | DIODE SS14 SHKTY 1A 40V DO214M | B | 1 | D3 |
| 88 | 32-600051-000 | DIODE TVS SMB12A 12V DO214AA | A | 1 | D2 |
| 89 | 32-600052-000 | DIODE TVS SMBJ5.0 5V DO214AA | A | 1 | D1 |
| 90 | 33-600032-000 | RESN CER 25MHZ 0.3% 3T 373113 | C | 1 | Y1 |

BOM Search Results



| | | | | | |
|---|---|---|---|---|---|
| 92 | 39-600091-000 | IND FERRITE BEAD POWER 1206 | B | 5 | L1 L2 L3 L4 L5 |
| 93 | 41-001321-003 | CONN PPHDR 16P2R ST HI-TEMP .045 TAIL | I | 1 | J1 |
| 94 | 42-000019-000 | CONN JMPR 2P 6mmX2.54mm CTR WHT | OB | 1 | J8 (1-2) |
| | 42-000018-002 | CONN JMPR 2P1R .1CT ST HDL WHT | | 1 | |
| 95 | 63-006364-000 | CONTACT SPRING | B | 4 | J11 J12 J13 J14 |
| 96 | 41-600042-000 | CONN CENTURY 54P COMBO SMTMULT | F | 1 | J2 J3 J8 |
| 100 | 63-001303-000 | LABEL BLANK 0.25 X 1.25 INCH | C | 1 | |
| 101 | 96-001875 | PCBA BARCODE PRINT SPEC. | EA | 0 | |
| 105 | 65-600840-000 | ARTWORK, REBEL / REBEL 2 ENTEK | A | 0 | |
| 106 | 61-600840 | PCBA, REBEL ENTEK DWG | A | 0 | |
| 107 | 68-600840-000 | SCHEMATIC, REBEL ENTEK | B | 0 | |

*This page took 6.301 seconds to process.*

Western Digital

Exhibit C



| | |
|---|---|
| PROJECT LEAD | |
| MGR CONTROLLER DEV | |

# WD70C10

## Device Specification

## I285s x 3.0

| REV | ECO | DESCRIPTION | DATE |
|---|---|---|---|
| A | WDC23672 | Initial Release | Smoraly 6/4/99 |

[redacted]

*WESTERN DIGITAL* CORPORATION

WD70C10
DEVICE SPECIFICATION

DOCUMENT NUMBER
96-107010-003